IN THE CLAIMS

Please cancel claim 1 and add new claims 35-48.

1-34. (Canceled).

35. (New) An information recording/readback circuit including:

a maximum likelihood sequence decoding circuit receiving a readback signal sequence from a recorded information medium as input, performing conversation into a readback data code series corresponding to said recorded information, and outputting results of said conversion; and

an error data detection/correction circuit receiving said converted readback data code series as input, checking for presence of decoding error data codes (readback data codes not corresponding to said recorded information) in said readback data code series, and correcting and outputting said detected decoding error data code as correct data code;

wherein partial code information (code position and code values) of said readback data code sequence detected by said error data detection/correction circuit is fed back to

said maximum-likelihood sequence decoding circuit as input; and

said maximum-likelihood sequence decoding circuit uses said partial code information and repeatedly converts said readback signal sequence into said readback data code sequence, and

wherein the repeated conversion in said maximum-likelihood sequence decoding circuit is done using the readback signal sequence corresponding to said recorded information again read from said recorded information medium (in retry mode).

36. (New) An information recording/readback circuit according to claim 35, wherein the said partial code information (code values) are represented by soft-output information with multi-level values.

37. (New) An information recording/readback circuit according to claim 35, wherein a code scrambling circuit is interposed between said maximum-likelihood decoder and said error data detection/correction circuit.

38. (New) An information recording/readback circuit according to claim 35 wherein said partial code information fed back as input to said maximum-likelihood sequence decoding circuit is formed from information (code position and code value) relating to data determined by said error data detection/correction circuit not to contain decoding error data (correct data code) in said readback data series, or information (code position and corrected code values) relating to data for which decoding error data was found and corrected by said error data detection/correction circuit.

39. (New) An information readback circuit as described in claim 35 wherein said repeated conversion to said readback data code sequence by said maximum-likelihood sequence decoding circuit is performed when said error data detection/correction circuit finds decoding error data codes in said readback data code sequence and correction of all said detected decoding error data codes is not possible.

40. (New) An information readback circuit as described in claim 35 wherein:

said readback data code series output from said maximum-likelihood sequence decoding circuit is divided into a plurality of code series; and

said data detection/correction circuit detects error data codes and performs corrections on each of said plurality of code series independently.

41. (New) An information readback circuit as described in claim 35 wherein:

said readback data code series output from said maximum-likelihood sequence decoding circuit is divided into a plurality of code series and sent separately into said a plurality of error data detector/corrector circuits for detection and correction of error data code, the results thereof being output from said error data detector/corrector circuits;

when one of said plurality of error data detection/correction circuits outputs an indication that decoding error data code in an incoming code series cannot be

corrected, a selector circuit selectively outputs part or all of code information from either an input signal for a data detection/correction circuit other than said error data detection/correction circuit or an output code series; and

output from said selector circuit is sent to said maximum-likelihood circuit.

42. (New) An information readback circuit as described in claim 35 wherein:

when said maximum-likelihood decoding circuit repeatedly performs conversion to a readback data code sequence, a partial code information fed back into said maximum-likelihood sequence decoding circuit is used and at least one of the following is performed:

(1) a code series not matching said partial code information is eliminated from maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected; and

(2) only code sequences matching said partial code information are set up as maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected.

43. (New) An information readback circuit as described in claim 35 wherein:

when said maximum-likelihood decoding circuit repeatedly performs conversion to a readback data code sequence, a partial code information fed back into said maximum-likelihood sequence decoding circuit is used and at least one of the following is performed:

(1) code sequences in which a code position (time) indicated in said code information being used does not contain a corresponding code value are eliminated from maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood

sequence) corresponding to said readback signal sequence is selected; and

(2) only code sequences in which a code position (time) indicated in said code information being used contains a corresponding code value are set up as maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected.

44. (New) An information readback circuit as described in claim 35 wherein:

said maximum-likelihood decoding circuit selects a readback data code sequence (maximum-likelihood code sequence) using a Viterbi algorithm;

when said maximum-likelihood decoding circuit repeatedly performs conversion to a readback data code sequence, a partial code information fed back into said maximum-likelihood sequence decoding circuit is used and at least one of the following is performed:

(1) code sequences in which a code position (time) indicated in said code information being used does not contain a corresponding code value are eliminated from maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected; and

(2) only code sequences in which a code position (time) indicated in said code information being used contains a corresponding code value are set up as maximum-likelihood candidate code sequences, degrees of likelihood for said maximum-likelihood candidate code sequences are compared, and a readback data code sequence (maximum-likelihood sequence) corresponding to said readback signal sequence is selected.

45. (New) An information readback circuit as described in claim 35 wherein:

said maximum-likelihood decoding circuit selects/estimates a readback data code sequence (maximum-

likelihood code sequence) using a predetermined code state transition diagram;

when said maximum-likelihood decoding circuit repeatedly performs conversion to a readback data code sequence, a partial code information fed back into said maximum-likelihood sequence decoding circuit is used and at least one of the following is performed:

(1) for a transition position (time) on said code state transition diagram corresponding to a code position (time) indicated by said code information being used, said readback data code sequence (maximum-likelihood code sequence) is selected/estimated using a code state transition diagram from which state transitions or code states not indicated by said code value are eliminated;

(2) for a transition position (time) on said code state transition diagram corresponding to a code position (time) indicated by said code information being used, said readback data code sequence (maximum-likelihood code sequence) is selected/estimated using a code state transition diagram in which only state transitions or code states indicated by said code value are left.

46. (New) An information readback circuit as described in claim 35 further comprising a code interleaving circuit changing a code sequence of said readback data code series before said error data detection/correction circuit detects decode error data and performs correction.

47. (New) An information readback circuit as described in claim 35 wherein:

said code interleaving circuit changing a code sequence of said readback data code series changes the sequence of said readback data code series using blocks of consecutive code having a predetermined length as units; and

said code interleaving circuit changing the sequence in said readback data code series so that consecutive code blocks are separated.

48. (New) An information readback circuit as described in claim 35 wherein said code length of said code block is no more than a code length of a code block serving as a

processing unit for detection and correction of decoded error data codes by said error data detecting/correcting means.